

**AMENDMENT TO THE SPECIFICATION:**

Please amend paragraph [022] on pages 8-9 as follows:

Input level shifter 50 further includes a complementary inverter (not numbered). The complementary inverter includes a third transistor 58 and a fourth transistor 60. In one embodiment according to the present invention, third transistor 58 includes a low-voltage PMOS transistor, and fourth transistor 60 includes a low-voltage NMOS transistor. Third transistor 58 includes a gate electrode 58-2, a first electrode 58-4 and a second electrode 58-6. Gate electrode 58-2 is coupled to a node M disposed between second transistor 54 and current source 56. First electrode 58-4 is coupled to a third power supply providing a voltage level of  $V_{AA}$  of, for example,  $(-10 + (3.6 \sim 5))$  V. Fourth transistor 60 includes a gate electrode 60-2, a first electrode 60-4 and a second electrode 60-6. Gate electrode 60-2 is coupled to node M. First electrode 60-4 is coupled to second electrode 58-6 of third transistor 58. Second electrode 60-6 is coupled to second power supply  $V_{EE}$ . A node [[M]]N disposed between third transistor 58 and fourth transistor 60 serves as an output terminal of input level shifter 50.